WHAT IS CLAIMED IS:

1. A memory device having a data line and a GMR storage circuit comprising:

at least one GMR storage cell that is coupled to the data line wherein the GMR storage cell magnetically stores a value indicative of the value of the data line upon receipt of a pre-selected storage signal;

a power down detector that detects when power to the memory device is being lost and generates the pre-selected storage signal, wherein the power down detector is adapted to provide a pre-selected storage signal that has a sufficient pulse width to change the magnetic state of the GMR storage cell when detecting that the power to the memory device is being lost.

2. The device of Claim 1, wherein the power down detector includes a charge storage device that stores charge during normal operation of the memory device and wherein the charge storage device provides the charge when the power is being lost to develop the pre-selected storage signal.

3. The device of Claim 2, wherein power down detector includes a pulse generating circuit that receives the charge and converts the charge into a pulse output signal having a pulse width.

4. The device of Claim 3, wherein the pulse generating circuit includes a logic gate having a first and second input and a delay circuit wherein the charge from the charge storage device is simultaneously applied directly to the first input of the logic gate and to the delay circuit and wherein the delay circuit provides an input signal to the second input of the logic gate a pre-selected time period after the application of the charge to the first input of the logic gate.

5. The device of Claim 4, wherein the logic gate provides the pulse output signal that changes from a first state to a second state upon receipt of the input signal on the first input and then changes back to the first state upon receipt of the input signal from the delay circuit on the second input such that the output from the logic gate comprises a pulse output signal that is in the second state for a pre-selected pulse width.

6. The device of Claim 5, wherein the logic gate comprises a NAND gate and the second state comprises a negative state.

7. The device of Claim 5, further comprising an output transistor that receives charge from the charge storage device and wherein the output transistor is activated by the pulse output signal such that the charge from the charge storage device is transmitted through the output transistor to the GMR device to produce the pre-selected storage signal.

8. The device of Claim 1, further comprising an isolation transistor interposed between the charge storage device and the power supply.

9. The device of Claim 8, further comprising an inverter that is coupled to the power supply so as to provide an output to the pulse generating circuit that is a rising edge signal in response to receiving a falling edge signal from the power supply indicative of the power to the memory device being lost.

10. The device of Claim 1, wherein the at least one GMR storage cell comprises at least one of a first magnetic layer that is magnetized in a first fixed direction, a second layer that can be magnetized in either the first fixed direction or a second direction that is opposite the first direction, and a spacing layer interposed between the first magnetic layer and the second magnetic layer.

11. The device of Claim 1, wherein the GMR storage circuit comprises a first conductive trace and second conductive trace that is substantially perpendicular to the first conductive trace, wherein the intersection point at which the first and second conductive traces is proximate to the at least one GMR storage cell.

12. The device of Claim 11, wherein a first component of the pre-selected storage signal is provided to the at least one GMR storage cell via the first conductive trace.

13. The device of Claim 12, wherein the GMR storage circuit comprises at least one access transistor interposed between the data line and the GMR storage cell, and wherein a second component of the pre-selected storage signal is provided to the at least one GMR storage cell via the second conductive trace upon activation by the data line.

14. An electronic device having a first and second input, the device comprising:

a pulse generating circuit that senses a power interrupt, receives a power interrupt signal at the first input, and generates a negative-level pulse signal upon sensing the power interrupt and upon receiving the power interrupt signal;

a transistor that receives the negative-level pulse signal and generates a positive-level pulse signal so as to produce a write current; and

a memory circuit that receives the write current and stores a volatile logic state sensed at the second input in at least one GMR storage element, wherein the at least one GMR storage element stores the volatile logic state in a non-volatile manner.

15. The device of Claim 14, wherein the pulse generating circuit includes a charge storage device that stores charge during normal operation of the electronic device and wherein the charge storage device provides the charge when the power is being lost to develop the power interrupt signal.

16. The device of Claim 15, wherein the pulse generating circuit receives the charge and converts the charge into the negative-level pulse signal having a pulse width.

17. The device of Claim 16, wherein the pulse generating circuit includes a logic gate having a first and second input and a delay circuit wherein the charge from the charge storage device is simultaneously applied directly to the first input of the logic gate and to the delay circuit and wherein the delay circuit provides an input signal to the second input of the logic gate a pre-selected time period after the application of the charge to the first input of the logic gate.

18. The device of Claim 17, wherein the logic gate provides the negative-level pulse signal that changes from a first state to a second state upon receipt of the input signal on the first input and then changes back to the first state upon receipt of the input signal from the delay circuit on the second input such that the output from the logic gate comprises the negative-level pulse signal that is in the second state for a pre-selected pulse width.

19. The device of Claim 17, wherein the logic gate comprises a NAND gate.

20. The device of Claim 17, the transistor receives charge from the charge storage device and wherein the transistor is activated by the negative-level pulse signal such that the charge from the charge storage device is transmitted through the transistor to the memory circuit so as to generate the write current.

21. The device of Claim 14, further comprising an isolation transistor interposed between the charge storage device and the power supply.

22. The device of Claim 14, further comprising an inverter that is coupled to the power supply so as to provide an output to the pulse generating circuit that is a rising edge signal in response to receiving a falling edge signal from the power supply indicative of the power to the memory device being lost.

23. The device of Claim 14, wherein the at least one GMR storage element comprises at least one of a first magnetic layer that is magnetized in a first fixed direction, a second layer that can be magnetized in either the first fixed direction or a second direction that is opposite the first direction, and a spacing layer interposed between the first magnetic layer and the second magnetic layer.

24. The device of Claim 14, wherein the GMR storage element comprises a first conductive trace and second conductive trace that is substantially perpendicular to the first conductive trace, wherein the intersection point at which the first and second conductive traces is proximate to the at least one GMR storage element.

25. The device of Claim 24, wherein a first component of the write current is provided to the at least one GMR storage element via the first conductive trace.

26. The device of Claim 25, wherein the memory circuit comprises at least one access transistor interposed between the second input and the GMR storage element, and wherein a second component of the write current is provided to the at least one GMR storage element via the second conductive trace upon activation by the second input.

27. An electronic device having a data line and a GMR storage cell, the device comprising:

an isolation transistor that senses a power failure and isolates a supply voltage from an operating voltage;

a charge storage device that stores the operating voltage and discharges the operating voltage when the power failure is sensed by the isolation transistor;

an inverter circuit that receives a power down signal and generates an inverted power down signal;

a pulse generating circuit that receives the inverted power down signal and generates an output pulse signal; and

a load transistor that receives the output pulse signal and generates a pre-selected storage signal that has a sufficient pulse width to change the magnetic state of the GMR storage cell when detecting that the power to the electronic device is being lost.

28. The device of Claim 27, wherein the electronic device further comprises a charge storage device that stores charge during normal operation of the electronic device and wherein the charge storage device provides the charge when the power is being lost to develop the pre-selected storage signal.

29. The device of Claim 28, wherein the pulse generating circuit receives the charge and converts the charge into the output pulse signal having a pulse width.

30. The device of Claim 29, wherein the pulse generating circuit includes a logic gate having a first and second input and a delay circuit wherein the charge from the charge storage device is simultaneously applied directly to the first input of the logic gate and to the delay circuit and wherein the delay circuit provides an input signal to the second input of the logic gate a pre-selected time period after the application of the charge to the first input of the logic gate.

31. The device of Claim 30, wherein the logic gate provides the pulse output signal that changes from a first state to a second state upon receipt of the input signal on the first input and then changes back to the first state upon receipt of the input signal from the delay circuit on the second input such that the output from the logic gate comprises a pulse output signal that is in the second state for a pre-selected pulse width.

32. The device of Claim 31, wherein the logic gate comprises a NAND gate and the second state comprises a negative state.

33. The device of Claim 31, wherein the load transistor receives charge from the charge storage device and wherein the load transistor is activated by the output pulse signal such that the charge from the charge storage device is transmitted through the load transistor to produce the pre-selected storage signal.

34. The device of Claim 27, wherein the isolation transistor is interposed between the charge storage device and the power supply.

35. The device of Claim 34, wherein the inverter circuit is coupled to the power supply so as to provide an output to the pulse generating circuit that is a rising edge signal in response to receiving a falling edge signal from the power supply indicative of the power to the electronic device being lost.

36. The device of Claim 27, wherein the at least one GMR storage cell comprises at least one of a first magnetic layer that is magnetized in a first fixed direction, a second layer that can be magnetized in either the first fixed direction or a second direction that is opposite the first direction, and a spacing layer interposed between the first magnetic layer and the second magnetic layer.

37. The device of Claim 27, wherein the electronic device further comprises a first conductive trace and second conductive trace that is substantially perpendicular to the first conductive trace, wherein the intersection point at which the first and second conductive traces is proximate to the at least one GMR storage cell.

38. The device of Claim 37, wherein a first component of the pre-selected storage signal is provided to the at least one GMR storage cell via the first conductive trace.

39. The device of Claim 38, wherein the GMR storage circuit comprises at least one access transistor interposed between the data line and the GMR storage cell, and wherein a second component of the pre-selected storage signal is provided to the at least one GMR storage cell via the second conductive trace upon activation by the data line.

40. A method of data retention during a power interrupt, the method comprising:

detecting the power interrupt;

developing a pulse signal having a sufficient pulse width to change the magnetic state of at least one GMR storage cell upon detecting the power interrupt;

supplying the developed pulse signal to the at least one GMR storage cell while simultaneously supplying a data input signal to the at least one GMR storage cell; and

magnetically storing the supplied input data signal in the at least one GMR storage cell using the developed pulse signal upon receiving the supplied pulse signal.